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Trellis based QC-LDPC convolution codes for low power decoders

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Abstract:- Now-a-days the communication should be more secure from source to destination. The reliable communication must be adequate for all the communications. The error correcting mechanism should be used for reducing the noise and the data loss in all the mediums. The sectional view could be easier to communicate without noise in all the data from source to destination. The decoder codes like LDPC codes are more secure and power efficient. The bit error rate is high for the high bit information in the input data. In this paper we are going to propose the novel LDPC code such as Trellis based Quasi cycle (TQC-LDPC) for lower complexity. This could be further reduced complexity and efficient communication for high granularity. The proposed QC-viterbi decoder can be effectively introduces here for the bit error rate transformation to the low density parity codes. This will occur in all the communication effectively with high security. The mode transferring from the association with all the convolution codes could be better. This will further implement in hardware also. The viterbi decoder algorithm having adequate information for the all high level input data's. this secure algorithm could be proposed over Xilinx ISE and modelsim simulation.

Keywords: *Lower complexity, LDPC convolution codes. Viterbi algorithm.*

1. INTRODUCTION

Convolution codes are most popular in data communication [2] for error calculating and then it could be further used for all high level applications [8]. The transferring rate must be noted from source to destination with high [11] input bit information. The communication between these nodes [7] are more secure with [4] high complexity the LDPC codes are to be changed as [3] per the input data transferring from the channel length [10] with the lower complexity.

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The communication between these channels having redundant bits while transmitting from all [13] the channels. Error control is necessary in all the applications [5] having the information from the data transferring. The codes for the high and low density must [8] be present as per the information in the source. The bit source can be equated [9] from the sectional view of the bit transfer to all the applications which is used in transmitter [11]. These convolution codes are non blocking codes and it can be related bit error rate [9].

The research process could be done in this algorithm can [8] be easily implemented in the technology such as FPGA, Application Specific Integration Circuit (ASIC) and Digital signal processing (DSP). All from the other studies [12] could be related to the lesser complexity based convolution can be adopted from the technology that can be varies. The information from [15] the parallel operation decoder units must be depending on the channel level modulation [11]. This could be when integrated into the highly integrated circuits with the environmental [6] data flow structure.

The low power viterbi decoder structure with low complexity [12] algorithm has been implemented with efficient bit error rate [2]. The parameters that can be followed from the conventional and the proposed method [1] can be varying from the each and every process. The method can be estimated [4] as per the derivation of all the technical flow within structure going to present the convolution codes [13]. The LDPC codes that can be employ as per the result for all the above terminology of the details [5] for the proposed method.

2. VITERBI DECODER

The viterbi architecture (Figure 1) for the decoding process basically consists of the following three blocks included as:

a. Branch metric unit (BMU)
b. Path metric unit (PMU)
c. Trace back unit (TBU)

d. Survival management unit (SMU)

This method can convert as the data information present in the inputs with the redundant bits. The process can be adopted from the technique for the high input bit rates can be easily adopted from the structured for the branch metric unit. The details can be modified as per the limit for the information can also to be given in that unit to be conveyed to the next unit. The communication between the path metric and the ACSU and SMU unit within the structure for the all data input bits. The parameters that can be transferred as per the redundant added in the input branch unit. The data that also to be with this cycle from the other output can take with the decoder for all the transformation from the technique to the searching units. The sectional view from all the output with the less bit error rate with reduced power consumption can be calculated.

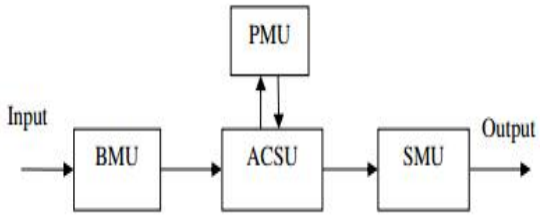

Figure 1: Viterbi decoding architecture

3. TRELLIS BASED QUASI CYCLE LDPC

In this quasi cycle convolution code can be transmitted with the block size of the 672 bit and the parity checker of all the transferred data's. The bit error rate information could be taken from the additional data present in the channel length of

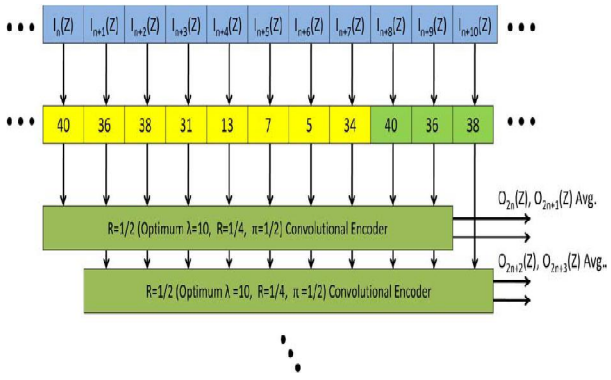

Figure 2. TQC-LDPC convolution encoder

the encoder. In this transmission the signal length and the process could be varied as per in the noise disturbances of the input bits (Figure 2). The code rate of the bits could be higher and also the rate can be measured as single and the multi method. In single bit code rate, the implementation process can be over process through the system and also it could be agreed as per the system management. In multi rate process the bit rate and the granularity could be high. By this process the function can be modified and also the bit error rate could be verified easily. In this elementary process the sectional details can be measured as P(i) where I is the polynomials present in the information and where Z is the number of rows. M is the number of bounds where we have to activate the BER

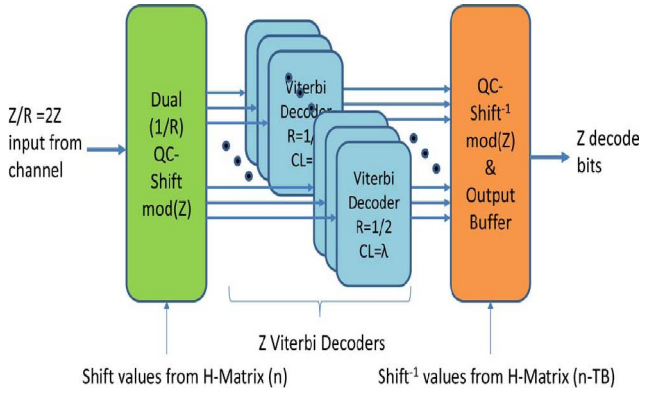

Figure 3. QC-viterbi decoder diagram

of the all information's. R=1/2 module can be split out from the each and every row of the input bit data's. the output buffer could be stored all the information temporarily from the Viterbi decoder of the LDPC codes.

Quasi cycle could be optimized from the unit where shift rows of the granularity can be adopted from the system. In case of WiGiG the parameter can be varied such as R_b =13/16 PCM with all of the error free control data of the system could be modified from the constraint length of the system management. The vertical and the horizontal process of the architectural view could be also implemented in hardware. When the Row Z could effectively added in the channel M=1 the noise present in the input data must also to be high. Then we have to reduce the power consumption resources and the bit error rate (Figure 3). Then we are going to end with the process for the increased data bit information to the granularity of bit error rate (BER) from the noisy channel. It can compute all the powerful polynomials and the reported elements from the all equations present in the quasi codes.

4. ADAPTIVE VITERBI ALGORITHM

The novel adaptive viterbi algorithm can be processed here to reduce the noise proportion of the metric paths from the control path. The valid selection from these units and the slots can be measured in the array of these paths. The branch metric generators BMG and the add compare/select units into the decision bias of the status. The memory units and the bit units could be processed from the decoder and the encoder architecture (figure 4).

Adaptive Viterbi Threshold Equation:

th = WC th – Threshold value

WC – Worst case branch metric value under error free condition

bm – branch metric node value

m - memory used to store branch metric value

if bm < th then m = bm else m = 0

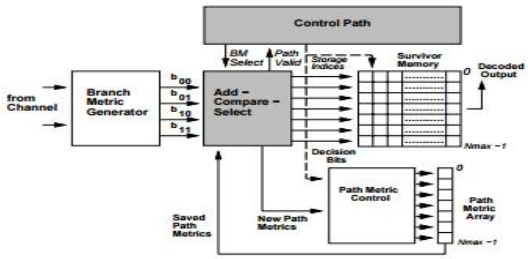

Figure 4: Adaptive viterbi decoder

The minimum stage from the architectural view of the all metrics is captured in the control path. The *dm* stages of the metrics in the development and the sum of the stages from the *dm+1* from the pictorial representation. The threshold conditions from the maximum units *Tm* into the representation for the memory of *Nmax*. The binary bits or the single code rate data's are the bit error rate to the reduced information. The decreased units into the *Nmax* of the decoder output as per in the survival path. The path metric control is the new path metric into the saved path.

The decoder accuracy can be measure in the path to be analyzed from the units to the captures into the *Nmax+1* unit for the architectural ports. The Bit error Rate can reduce as per the data's from the input bits. The decision bias of the representation of the all data with noisy length of the valid path could be recognized. The decoder accuracy can be eliminated in the noisy length of the channel with the coded signal of the decoder path. The main advantage is the signals with error bits of the status into reduced signals. The sectional view as per the rate of the data bit into the signals for single and the multi rate of the desired increase noise. The channel constraint length to be adequate of the all data information present into the bit error rate to be calculated. The branch metric unit to be assigned from the all bit functional rate can be measured maximum number of bits. The channel must be long and the input bit rate must be high bit rate in the adaptive viterbi algorithm of the output decoder. The granularity form the bit error rate must be recognized into the weak signals of the adaptive process of the related views. The memory can be used as per in the data rate to be analyzed properly with high bit rate.

5. SIMULATION RESULTS

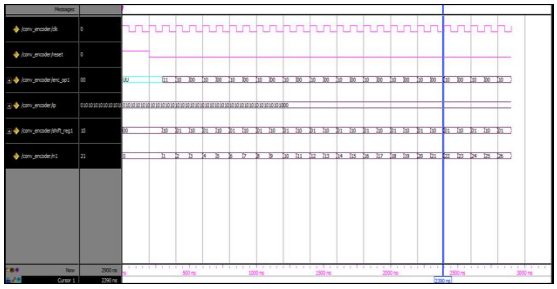

Fig 5: Simulation for convolution encoder

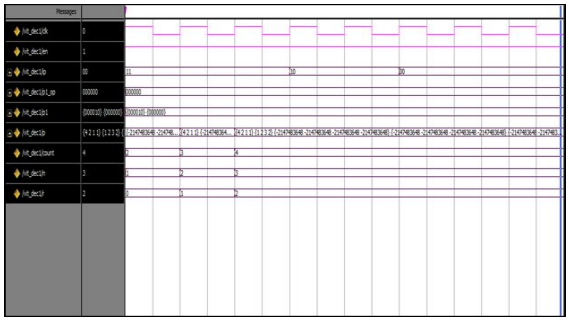

Fig 6: Simulation for viterbi decoder

The novel Adaptive algorithm with LDPC code architecture simulation can be done through the Xilinx ISE using HDL. The data address bit verification can also to be done through this simulation and the waveform could be verified by using the MODELSIM (Figure 5-10).

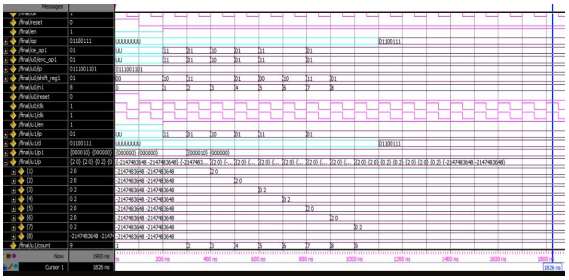

Fig 7: Simulation for convolution Combination of Convolutional Encoder and Viterbi Decoder

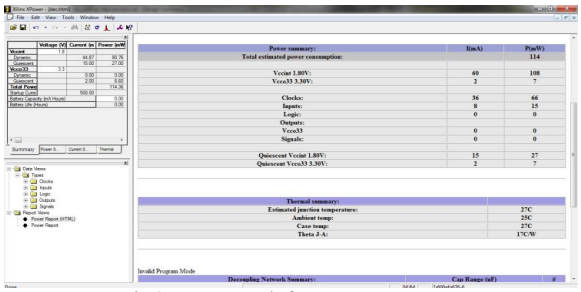

Fig 8: Power result for QCL-LDPC

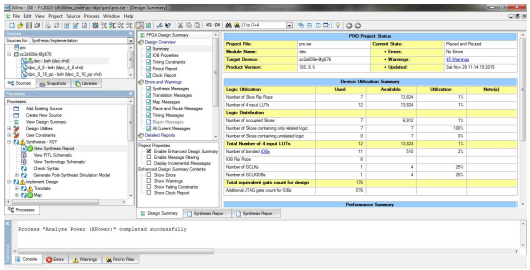

Fig 9:Area report for QCL-LDPC

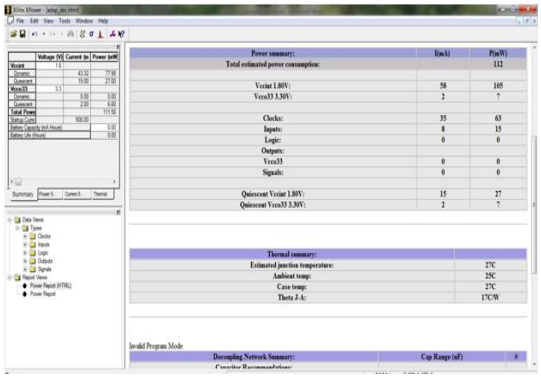

Fig 10: Power result for Adaptive viterbi decoder

6. PERFORMANCE COMPARISON

Table 1 shows the result comparison of the conventional and the novel convolution viterbi decoder algorithm. By comparing this result we can identify that the proposed novel algorithm has been efficient performance in power, area and the delay. This can be feasibly implemented in the hardware also.

TABLE 1
Performance evaluation

Parameters / Types	Delay(ns)	Power(mW)	Area(Gate count)
Belief Propagation	6.237	162	565
QC-Viterbi decoder	5.422	114	176
Adaptive QC-Viterbi decoder	4.817	112	92

7. CONCLUSION

The proposed architecture has been comparatively analyzed with the functional blocks of the conventional decoder with its bit error rate. The transformation of the decoder has been analyzed as per the results in the hardware implementation of the system. The method can be recognized from this process can be taken away from the result comparison of the conventional and the proposed system. The testing level convention between the transformations of these bits indicates the area and the power efficient technology. This could be added in the parallel design of the adaptive decoder with the high bit rate also to be accept from the system variations in the performance based view.

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